# DESCRIPTION

CAPACITANCE DETECTION CIRCUIT AND CAPACITANCE DETECTION
METHOD

## Technical Field

The present invention relates to a circuit that detects electrostatic capacitance and particularly to a circuit that outputs a signal corresponding to variant component of very small electrostatic capacitance.

## Background Art

A capacitance detection circuit 10 shown in FIG. 1 conventionally exists as a detection circuit of a capacitive sensor of which electrostatic capacitance (hereinafter, referred to simply as "capacitance") changes corresponding to a variance in physical quantity.

This capacitance detection circuit 10 is a circuit that outputs a voltage signal corresponding to capacitance of a capacitive sensor Cs and is constructed of: the capacitive sensor Cs; an input protection circuit 11; a resistor Rh; a buffer amplifier 12; a signal wire 13 that connects the capacitive sensor Cs and the buffer amplifier 12; and the like. (Refer to, for example, Laid-open Japanese patent application No. 5-335493 as an input protection circuit.)

Voltage Vb is applied to an electrode of the capacitive sensor Cs and other electrode is connected to an input terminal of the buffer amplifier 12 via the signal wire 13. The input protection circuit 11 is a circuit that clamps high voltage such as static electricity diving into the signal wire 13 to supply voltage and is composed of diodes Dp and Dm connected between the signal wire 13 and positive power supply (+Vdd) and negative power supply (−Vdd).

The conventional capacitance detection circuit 10 like this acts as follows.

Now, suppose that parasitic capacitance (stray capacitance) of the signal wire 13 is $C_i$, and input voltage $V_{in}$ of the buffer amplifier 12 is divided voltage of voltage $V_b$ applied to the capacitive sensor $C_s$ and determined by the capacitive sensor $C_s$ and the parasitic capacitance $C_i$.

$V_{in} = V_b \cdot (1/j\omega C_i) / (1 / j\omega C_s + 1 /j\omega C_i)$

By the way, the voltage gain of the buffer amplifier 12 being 1,

$V_{out} = V_{in}$ holds.

Therefore, when $V_{in}$ is deleted in the above two equations, output voltage $V_{out}$ is:

$V_{out} = V_b \cdot C_s / (C_s + C_i)$

Here, suppose that capacitance of the capacitive sensor $C_s$ is represented by adding a capacitance component that depends on a variance in physical quantity (variant capacitance $\Delta C$) and a capacitance component that does not depend on a variance in physical quantity (reference capacitance $C_d$), in other words, suppose that it is represented by

$C_s = C_d + \Delta C$

The above-mentioned output voltage $V_{out}$ is:

$V_{out} = V_b \cdot (C_d + \Delta C) / (C_d + \Delta C + C_i)$

Here, when $V_b$ is direct voltage, only AC component $V_o$ of the output voltage $V_{out}$ corresponding to a variance in physical quantity is a final signal. Therefore, the AC component $V_o$ is:

$V_o = V_b \cdot \Delta C / (C_d + \Delta C + C_i)$ -- (Equation 1)

(Here, it is possible to state that $V_o$ is component that depends on a temporal variance in physical quantity, "for example, $\Delta C$".)

As is apparent from the above Equation 1, to improve sensitivity of the capacitance detection circuit like this, it is

preferable to diminish or null the parasitic capacitance Ci because $\Delta C$, Cd and Vb are constant.

It is not easy, however, to diminish the parasitic capacitance Ci.

5 FIG. 2 is an equivalent circuit diagram when the capacitance detection circuit 10 shown in FIG. 1 operates normally (when diodes Dp and Dm are reversely biased.) Here, capacitance of diode Dp and capacitance of diode Dm (depletion layer capacitance when being reversely biased) are illustrated as capacitors Cdp and Cdm, 10 respectively and input capacitance of the buffer amplifier 12 is illustrated as a capacitor Cg. The parasitic capacitance Ci is a total value of capacitance of these capacitors, Cdp, Cdm and Cg:

$Ci = Cdp + Cdm + Cg$

All of them, however, are parasitic capacitance produced by an 15 essential circuit.

Here, if it is possible to form the whole capacitance detection circuit 10 with a one-tip IC, it is possible to reduce the parasitic capacitance Ci substantially without providing the input protection circuit 11. However, when it is necessary to produce a product by 20 assembling two or more kinds of parts or to implement a capacitive sensor Cs and a detection circuit at positions far apart or the like, it is inevitable to implement a capacitance detection circuit with a structure in which the capacitive sensor Cs and the detection circuit are separated. It is, therefore, unavoidable to provide the input 25 protection circuit 11 in the input stage of the buffer amplifier 12. Consequently, parasitic capacitance caused by the input protection circuit 11 is added and there is a problem that the sensitivity of the capacitance detection circuit deteriorates.

30 **Disclosure of Invention**

Thus, the present invention is made considering the problem like this and aims to provide a capacitance detection circuit that

contains an input protection circuit and has high sensitivity.

To achieve the above-mentioned object, the capacitance detection circuit according to the present invention is skillfully designed to cancel capacitance of the diodes that form the input
5  protection circuit.

In other words, the capacitance detection circuit according to the present invention is a capacitance detection circuit comprising: a first buffer amplifier unit connected to a capacitor to be detected via a signal wire; a first diode and a second diode connected in series
10  between the signal wire and a first power supply; and a third diode and a fourth diode connected in series between the signal wire and a second power supply, wherein an output terminal of the first buffer amplifier unit is connected to a first junction point of the first diode and the second diode and to a second junction point of the third
15  diode and the fourth diode.  Hereby, since the both ends of the first and the third diodes connected to the signal wire become same potential, the capacitance of the diodes is cancelled; parasite capacitance becomes smaller; and the sensitivity of the capacitance detection circuit becomes large.

20  Here, the first power supply is preferably positive potential and normally the positive power supply in the circuit is used. Additionally, the second power supply is preferably negative potential and normally the negative power supply in the circuit or the ground is used.  The first buffer amplifier unit can be anything
25  with the function of a buffer amplifier.  The voltage gain of the first buffer amplifier is most preferably 1 but a value other than that is possible.  Furthermore, the bias voltage applied to the capacitor to be detected may be AC or DC or AC over DC.

Moreover, it is acceptable that the output terminal of the first
30  buffer amplifier unit is connected to the first junction point via a first capacitance and to the second junction point via a second capacitance, the first junction point is connected to a point having

potential between potential of the first power supply and potential of the signal wire via a first resistor, and the second junction point is connected to a point having potential between potential of the second power supply and potential of the signal wire via a second

5    resistor.    At this time, it is preferable that the first resistor and the first capacitor are, respectively, a resistance value and a capacitance value that pass frequency elements of output signals from the first buffer amplifier unit corresponding to variant capacitance of the capacitor to be detected and AC component of

10    biased voltage added to said capacitor to be detected, and the second resistor and the second capacitor are, respectively, a resistance value and a capacitance value that pass frequency elements of output signals from the first buffer amplifier unit corresponding to variant capacitance of the capacitor to be detected

15    and AC component of biased voltage added to said capacitor to be detected.    Hereby, since the output terminal of the first buffer amplifier unit is connected in AC with the first and the second junction points and the both ends of the first diode and the third diode connected to the signal wire are same potential in AC, the

20    capacitance of the diodes is cancelled; parasite capacitance becomes smaller; and the sensitivity of the capacitance detection circuit becomes large.

        Additionally, it is acceptable that a second buffer amplifier unit is connected between (i) a junction point of the first resistor and

25    the first capacitor and (ii) the first junction point and a third buffer amplifier unit is connected between (i) a junction point of the second resistor and the second capacitor and (ii) the second junction point. Here, it is preferable that each voltage gain of the first to third buffer amplifier units is set so that potential of the first junction point and

30    potential of the second junction point are same as potential of the signal wire.    It is further preferable that the voltage gain of all the first to third buffer amplifier units is 1.    Hereby, the both ends of the

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first diode and the third diode are kept at the same potential more securely.

Moreover, it is preferable that the first buffer amplifier unit includes a MOSFET as an input circuit, a gate of the MOSFET is connected to an input terminal of the first buffer amplifier unit, and a substrate of the MOSFET is connected to an output terminal of the first buffer amplifier unit. Hereby, the input capacitance of the first buffer amplifier unit is cancelled and the sensitivity of the capacitance detection circuit improves.

Additionally, it is acceptable that the capacitance detection circuit further includes: a testing terminal for an input of a testing signal; a testing capacitor and a switch connected in series between the input terminal of the first buffer amplifier unit and the testing terminal. Hereby, when the capacitance detection circuit is realized as a circuit divided from the capacitor to be detected, it is possible to conduct an operation test with the capacitance detection circuit itself as if the capacitor to be detected is connected even though the capacitor to be detected is not connected.

By the way, the present invention can be realized not only as the capacitance detection circuit like this but also as a capacitance detection method that improves the sensitivity by canceling the capacitance of diodes in the input protection circuit.

The capacitance detection circuit according to the present invention cancels the capacitance of the diodes connected to the signal wire among the diodes that make up the input protection circuits, and therefore the parasitic capacitance of the signal wire diminishes and the sensitivity of the capacitance detection circuit significantly improves.

Moreover, by applying, to the diodes of the input protection circuits, frequency elements of output signals from the buffer amplifier units that make up the capacitance detection circuit corresponding capacitance variance of the capacitive sensor and AC

component of bias voltage added to said capacitor to be detected, voltage of the both ends of the diodes connected to the signal wire among the diodes that make up the input protection circuit become same in AC and the capacitance is cancelled. And therefore, the parasitic capacitance of the signal wire becomes smaller and the sensibility of the capacitive sensor as a capacitance detection circuit that detects capacitance variance improves significantly.

Additionally, connecting a substrate of a MOSFET and an output terminal of the buffer amplifier in the input stage of the buffer amplifier cancels the input capacitance of the buffer amplifier. And therefore, the parasite capacitance of the signal wire diminishes and the sensibility of the capacitance detection circuit improves.

Further, by incorporating a testing capacitor and a switch in the capacitance detection circuit, it is possible to make a state that the capacitive sensor is connected to the capacitance detection circuit even if the capacitive sensor is not connected. And therefore, it is possible to conduct an action test of the circuit. On the other hand, when an action test is not conducted, it is possible to connect the testing capacitor between the input terminal and the output terminal of the buffer amplifier unit.

**Brief Description of Drawings**

FIG. 1 is a circuit diagram of a conventional capacitance detection circuit.

FIG. 2 is a circuit diagram of an equivalent circuit of the capacitance detection circuit shown in FIG. 1.

FIG. 3 is a circuit diagram of the capacitance detection circuit according to the First Embodiment of the present invention.

FIG. 4 is a circuit diagram of an equivalent circuit of the capacitance detection circuit shown in FIG. 3.

FIG. 5 is a circuit diagram of the capacitance detection circuit according to the Second Embodiment of the present invention.

FIG. 6 is a circuit diagram of an equivalent circuit of the capacitance detection circuit shown in FIG. 5.

FIG. 7 is a circuit diagram in which signal voltage is written on the equivalent circuit shown in FIG. 6. FIG. 7A is a circuit diagram when the circuit is in a steady state while FIG. 7B is a circuit diagram when the circuit is in a variant state.

FIG. 8 is a circuit diagram of a capacitance detection circuit in which two buffer amplifiers are added to the capacitance detection circuit shown in FIG. 5.

FIG. 9 is a circuit diagram in which a MOSFET substrate constructing an input stage of a buffer amplifier and the output terminal of the buffer amplifier are connected.

FIG. 10 is a circuit diagram in which a testing capacitor is added to a capacitance detection circuit.

FIG. 11A and FIG. 11B are circuit diagrams showing an example of a buffer amplifier.

## Best Mode for Carrying Out the Invention

The embodiments of the present invention are explained below in detail using drawings.

(The First Embodiment)

FIG. 3 illustrates a circuit diagram of a capacitance detection circuit 20 according to the First Embodiment as an example of the present invention.

This capacitance detection circuit 20 is a circuit that outputs a voltage signal corresponding to capacitance of a capacitive sensor Cs and is constructed of the capacitive sensor Cs, an input protection circuit 21, a resistor Rh, a buffer amplifier 12, a signal wire 13 that connects the capacitive sensor Cs and the buffer amplifier 12 and the like. The signal wire 13 is connected to a power supply Vh via a pull-up resistor Rh and through which DC is

fixed. The buffer amplifier 12 is an impedance converter of which input impedance is high, output impedance is low and voltage gain is 1. Compared with the conventional capacitance detection circuit 10 shown in FIG. 1, it is different in the construction of the input

5  protection circuit 21, the point that the buffer amplifier 12 and the input protection circuit 21 are connected and the like. The same components as the conventional capacitance detection circuit are given the same reference numbers in the drawings, their explanation is omitted and the only different points are explained

10  below.

The input protection circuit 21 is constructed of: two diodes Dp1 and Dp2 that are connected so that electric current between the signal wire 13 and the positive power supply (+Vdd) flows in the direction from the signal wire 13 to the positive power supply

15  (+Vdd); and two diodes Dm1 and Dm2 that are connected so that electric current between the signal wire 13 and the negative power supply (−Vdd) flows in the direction from the negative power supply (−Vdd) to the signal wire 13.

Then, the output terminal of the buffer amplifier 12 is

20  connected not only with the junction point 21a between the diode Dp1 and the diode DP2 of the input protection circuit 21 but also with the junction point 21b between the diodes Dm1 and Dm2.

The capacitance detection circuit 20 constructed as described above acts as follows.

25  FIG. 4 is a circuit diagram of an equivalent circuit of the capacitance detection circuit 20 shown in FIG. 3. Here, the capacitance of the diodes Dp2 and Dm1 is illustrated as the capacitors Cdp and Cdm, respectively and the input capacitance of the buffer amplifier 12 is illustrated as the capacitor Cg.

30  Focusing attention on the capacitor Cdp, its both ends have the same electric potential because they are connected to the input terminal and the output terminal of the buffer amplifier 12.

Similarly, the both ends of the capacitor Cdm have the same electric potential. In other words, both of these capacitors Cdp and Cdm have the same electric potential in their both ends; accumulated charge is zero; and the capacitance Cdp and Cdm are zero in appearance. This is easily understandable because in the relationship among capacitance C of a capacitor, accumulated charge Q and voltage V between the both terminals:

$$Q = C \cdot V$$

when V= 0, Q=0, in other words, accumulated charge is 0 and equals, in appearance, to the case when the capacitance C is zero.

As is described above, it is possible to ignore the capacitance of two diodes Dp2 and Dm1 connected to the signal wire 13 (the capacitors Cdp and Cdm). Therefore, the parasitic capacitance Ci of the signal wire 13 is only the capacitor Cg, that is:

$$Ci = Cg$$

Consequently, compared with the parasitic capacitance Ci (=Cdp + Cdm + Cg), the capacitive component caused by the input protection circuit is reduced and therefore the sensibility of the capacitance detection circuit 20 improves by the reduced component. In other words, Ci included in the denominator of the above Equation 1 diminishes substantially and the circuit gain

$$\Delta C / (Cd + \Delta C + Ci)$$

is substantially larger than the conventional one.


(The Second Embodiment)

FIG. 5 illustrates a circuit diagram of a capacitance detection circuit 30 according to the Second Embodiment that is an example of the present invention.

This capacitance detection circuit 30 is a circuit that outputs a voltage signal corresponding to capacitance of a capacitive sensor Cs and is constructed of the capacitive sensor Cs, an input protection circuit 31, a resistor Rh, a buffer amplifier 12, a capacitor

Cp, a capacitor Cm, a signal wire 13 that connects the capacitive sensor Cs and the buffer amplifier 12 and the like. Compared with the capacitance detection circuit 20 shown in FIG. 3, it is different in the point that two capacitors Cp and Cm and two resistors Rp and Rm are added. The same components as the capacitance detection circuit 20 of the First Embodiment are given the same reference numbers in the drawings, their explanation is omitted and the only different points are explained below.

The resistor Rp is connected between fixed voltage Vp and a junction point 31a of a diode Dp1 and a diode Dp2 in the input protection circuit 31, and the capacitor Cp is connected between the output terminal of the buffer amplifier 12 and the junction point 31a. Similarly, the resistor Rm is connected between fixed voltage Vm and a junction point 31b of a diode Dm1 and a diode Dm2, and the capacitor Cm is connected between the output terminal of the buffer amplifier 12 and the junction point 31b.

The capacitor Cp and the resistor Rp construct a high pass filter with the output voltage of the buffer amplifier 12 as an input and the junction point of them as an output. And the capacitance value and the resistor value are set to be constants when a signal passes in the frequency band corresponding to variant capacitance $\Delta C$ of the capacitive sensor Cs and voltage Vb (an alternate current component) of bias supply. Similarly, as for the capacitor Cm and the resistor Rm, the capacitance value and the resistor value are set to be constants when a signal passes in the similar frequency band. Consequently, the alternate current component of the output voltage of the buffer amplifier 12 is applied to the junction point 31b of the input protection circuit 31 across the capacitor Cm.

Fixed voltage Vp is: value between voltage Vh of the signal wire 13 and positive power supply (+Vdd); and DC potential to bias the diodes Dp1 and Dp2 so that both of them are reverse-biased in normal operation. Similarly, fixed voltage Vm is: value between

voltage Vh of the signal wire 13 and negative power supply ($-$Vdd); and DC potential to bias the diodes Dm1 and Dm2 so that both of them are reverse-biased in normal operation.

The capacitance detection circuit 30 constructed as described above acts as follows.

FIG. 6 is a circuit diagram of an equivalent circuit of the capacitance detection circuit 30 shown in FIG. 5. Here, the capacitance of the diodes Dp2 and Dm1 is illustrated as the capacitors Cdp and Cdm, respectively and the input capacitance of the buffer amplifier 12 is illustrated as the capacitor Cg.

AC voltage component in the signal wire 13 is outputted from the buffer amplifier 12, passes through the capacitors Cp and Cm and is applied to the junction points 31a and 31b of the input protection circuit 31. In other words, focusing attention on the AC component, each of the capacitors Cdp and Cdm has the same potential in the both terminals and therefore the capacitance Cdp and Cdm is zero in appearance, similarly to the First Embodiment.

As is described above, since it is possible to ignore the capacitance of two diodes Dp2 and Dm1 (the capacitors Cdp and Cdm) connected to the signal wire 13, the parasitic capacitance Ci of the signal wire 13 is only the capacitor Cg and the same effect as the First Embodiment is achieved.

The explanation of the above operation using an analytical expression is as follows.

FIG. 7A is a circuit diagram on which voltage value of each point is written when the capacitance detection circuit 30 is in steady state, in other words, when the capacitive sensor Cs equals to a constant value Cd (variant capacitance $\Delta C=0$). Here, voltage Vb is DC. In other words, the voltage of the signal wire 13 is Vh; the output voltage of the signal wire is Vh; the voltage at the junction point 31a of the input protection circuit 31 is Vp; and the voltage at the junction point 31b of the input protection circuit 31 is

Vm.

On the other hand, FIG. 7B is a circuit diagram on which voltage value of each point is written when the capacitance of the capacitive sensor Cs of the capacitance detection circuit 30 is variant. In other words, the voltage of the signal wire 13 is (Vsig + Vh); the output voltage of the buffer amplifier 12 is (Vsig + Vh); the voltage at the junction point 31a of the input protection circuit 31 is (Vsig + Vp); and the voltage at the junction point 31b of the input protection circuit 31 is (Vsig + Vm).

Here, if the resistor Rh and the input resistor of the amplifier 12 are extremely high and the charge amount of the signal wire 13 is stored, the charge amount Q1 of the signal wire 13 in the steady state shown in FIG. 7A equals to the charge amount Q2 of the signal wire 13 in the variant state shown in FIG. 7B.

Here, the charge amount Q1 of the signal wire 13 in the steady state shown in FIG. 7A is:

$$Q1 = Cd \cdot (Vh - Vb) + Cdp \cdot (Vh - Vp) + Cdm (Vh - VM) + Cg \cdot Vh$$

On the other hand, the charge amount Q2 of the signal wire 13 in the variant state shown in FIG. 7B is:

$$Q2 = (Cd + \Delta C) \cdot (Vsig + Vh - Vb) + Cdp \cdot (Vsig + Vh - Vsig - VP) + Cdm (Vsig + Vh - Vsig - Vm) + Cg \cdot (Vsig + Vh)$$

And then, Q1 = Q2 is satisfied. With these equations, the signal component Vsig corresponding to a variance in the capacitance of the capacitive sensor Cs is represented by:

$$Vsig = (\Delta C / (Cd + \Delta C + Cg)) \cdot (Vb - Vh)$$

From these equations, it is apparent that the AC component of an output signal of the buffer amplifier 12 is not effected by the capacitance of the two diodes Dp2 and Dm1 (the capacitors Cdp and Cdm) of the input protection circuit 31. In other words, the parasitic capacitance Ci of the signal wire 13 is, in appearance, only the capacitor Cg and the sensibility is larger than the conventional.

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The capacitance detection circuit according to the present invention is explained using two embodiments but the present invention is not limited by these embodiments.

For example, it is acceptable that voltage Vb of bias supply is AC or AC over DC. And it is also acceptable, like a capacitance detection circuit 40 shown in FIG. 8, that buffer amplifiers 42 and 43 are connected from the junction point between two diodes and the output terminal of the buffer amplifier 12 via the capacitor Cp or the capacitor Cm. This capacitance detection circuit 40 is equivalent to a circuit to which impedance converters of which input impedance is high, output impedance is low and voltage gain is 1 (buffer amplifiers 42 and 43, respectively) are inserted between the junction point 31a of the capacitance detection circuit 30 according to the Second Embodiment and the resistor Rp and between the junction point 31b and the resistor Rm. Hereby, not only the input protection circuit 41 is separated from output load of the buffer amplifier 12 but voltage is supplied to the junction points 41a and 41b of the input protection circuit 41 via the buffer amplifiers 42 and 43. Therefore, it is more securely possible to hold the potential of the both terminals of the capacitors Cdp and Cdm at the same potential.

Additionally, as is shown in a circuit diagram in FIG. 9, when an input terminal is connected to a MOSFET gate in a circuit inside the buffer amplifier 12, the input capacitance of the buffer amplifier 12 (the capacitor Cg) is gate capacitance of the MOSFET, most of which is capacitance between a gate and a substrate. Therefore, in a case like this, it is acceptable to connect the substrate of the MOSEFT and the output terminal of the buffer amplifier 12. Hereby, the capacitance between the gate and the substrate is cancelled, the parasitic capacitance Ci diminishes and the sensibility of the capacitance detection circuit improves.

Furthermore, when a capacitance detection circuit excluding

the capacitive sensor Cs can be realized by a one-chip IC, a breadboard and the like, it is acceptable to add a circuit to test the capacitance detection circuit as is shown in a circuit diagram in FIG. 10. In the circuit diagram in FIG. 10, the input terminal of the buffer amplifier 12 is connected with a testing PAD (an electrode terminal of the IC) 52 via a testing capacitor 50 and a switch 51; and a control terminal of the switch 51 is connected to a switching PAD 53 (or a switching control circuit). With the construction like this, at a time of test, by applying predetermined first voltage from the switching PAD 53; connecting the switch 51 with the testing PAD 52; and making them in a testing state, the capacitive sensor (the testing capacitor 50) is in a state of being connected to the capacitance detection circuit. As a result, it is possible to test the capacitance detection circuit by inputting a testing signal to the testing PAD 52 or the like. On the other hand, after the test completes, by applying predetermined second voltage from the switching PAD 53; connecting the switch 51 with the output terminal of the buffer amplifier 12; and making the two terminals of the testing capacitor 50 have the same potential, it is possible that deterioration of the sensibility will not occur.

Additionally, it is acceptable to the buffer amplifiers 12, 42 and 43 are constructed of voltage follower by an operational amplifier shown in FIG. 11A or of a circuit using MOSFET shown in FIG. 11B.

Furthermore, when phase difference occurs at voltage of the both ends of the capacitors Cdp and Cdm, it is acceptable to adjust by inserting a phase compensation circuit on a loop circuit from one end to the other end of the capacitors Cdp and Cdm so that the phase difference does not occur. Or it is also acceptable to make phase compensation and adjust a passing band at the same time by when the resistors Rp and Rm are variable resistance and the capacitors Cp and Cm are variable capacitance in the capacitance

detection circuit 30 according to the Second Embodiment.

**Industrial Applicability**

The present invention is used as a capacitance detection
circuit and particularly as a circuit that outputs a signal according to
variant component of very small electrostatic capacitance, for
example, a detection circuit of a capacitive sensor such as a
capacitance microphone of which capacitance changes according to
a variance in physical quantity.